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EXAMINER

PATEL, DHARTI HARIDAS

ART UNIT

PAPER NUMBER

2836

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Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|----------------------------------|--|
| Office Action Summary | Application No. 10/725,852 | Applicant(s) WU ET AL. | |
| | Examiner Dharti H. Patel | Art Unit 2836 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 23 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,682,993. Although the conflicting claims are not identical, they are not patentably distinct from each other. Claim 23 of the application is recited in patented claim 1. Claim 23 of the application is broader in scope than claim 1 of the patent in that claim 23 does not recite the NMOS device with a special diffusion, under and around said device normal drain region of opposite dopent than said normal drain region and a resistor. However, it would have been

Art Unit: 2836

obvious to those skilled in the art at the time the invention was made to provide the protection circuit without the NMOS regions as claimed to provide a simpler circuit which does not require the same level of ESD protection. The product claims recite structure of the device used in the method claims and are obvious in view of the method claims.

3. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claim 24/23 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,682,993. This is a double patenting rejection.

Claim Objections

5. Claims 12-22 are objected to because the claim limitations [Claim 12, lines 10-13, multiple regions of a third dopent type and a special fourth dopent region] are not supported by the material in the Specification. The limitations of claim 12 should be addressed to account for this.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. With respect to claim 23, the acknowledged prior art [Fig. 1A] teaches a method of forming a protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said method comprising connecting source region of a used PMOS device [Fig. 1A, PU1] and the source and gate of an unused PMOS device [Fig. 1A, PD1] to a first voltage source [Fig. 1A, Vcc]; connecting the drains of said used [Fig. 1A, PU1] and unused [Fig. 1A, PD1] PMOS devices to said active devices input/output pad [Fig. 1A, 8]; connecting the drain of said used PMOS device [Fig. 1A, PU1] to a drain of a first used NMOS device [Fig. 1A, NU1], and the drain of said unused PMOS device [Fig. 1A, PD1] to a drain of a first unused NMOS device [Fig. 1A, ND1]; connecting the gate of said used PMOS device [Fig. 1A, PU1] and the gate of a second used NMOS device [Fig. 1A, NU2] to separate logic signal lines; connecting the gates of said first used [Fig. 1A, NU1] and said first unused ND1 NMOS devices to said first voltage source [Fig. 1A, Vcc]; connecting the source of said first used NMOS device [Fig. 1A, NU1] to the

drain of said second used NMOS device [Fig. 1A, NU2] and connecting source of said first unused NMOS device [Fig. 1A, ND1] to the drain of a second unused NMOS device [Fig. 1A, ND2]; connecting the source of said second used NMOS device [Fig. 1A, NU2] and the source and gate of said second unused NMOS device [Fig. 1A, ND2] to a second voltage source [Fig. 1A, Vss]; and connecting said ESD protection discharging means [Fig. 1A, 7] for discharging ESD energy appearing between and further directly connected to said first [Fig. 1A, Vcc] and second [Fig. 1A, Vss] voltage source.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-2, 4-11, and 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Chen et al., Patent No. 6,858,900. With respect to claim 1, applicant's prior art [Fig. 1A] teaches a protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said circuit comprising at least one switching circuit string [Fig. 1A, 6] composed of a first [Fig. 1A, NU1] and second [Fig. 1A, NU2] NMOS device and a PMOS device

[Fig. 1A, PU1], wherein the gate of said first NMOS device [Fig. 1A, NU1] is connected to a first voltage source [Fig. 1A, Vcc] and the drain element of said first NMOS device [Fig. 1A, NU1] is connected to said active devices input/output signal pad [Fig. 1A, 8] and to the drain element said PMOS device [Fig. 1A, PU1], and the source of said first NMOS device [Fig. 1A, NU1] is connected to the drain element of said second NMOS device [Fig. 1A, NU2] and the gates of said second NMOS [Fig. 1A, NU2] and said PMOS [Fig. 1A, PU1] are connected to an internal circuit [Fig. 1A, 4] and the source of said second NMOS [Fig. 1A, NU2] is connected to a second voltage source [Fig. 1A, Vss], and the source of said PMOS [Fig. 1A, PU1] is connected to a first voltage source [Fig. 1A, Vcc]; and a protection discharging means [Fig. 1A, 7, discharging NMOS device] for discharging ESD energy appearing between said first [Fig. 1A, Vcc] and said second [Fig. 1A, Vss] voltage source, and the drain of said discharging NMOS device is directly connected to said first voltage source [Fig. 1A, Vcc], and the source of said discharging NMOS device is directly connected to said second voltage source [Fig. 1A, Vss]. However, the prior art fails to teach or suggest a protection discharging means comprising a discharging NMOS device with a first and a second drain diffusion.

Chen et al. teaches electrostatic discharge protection devices that have islands and breakdown-enhanced layers. Chen et al. teaches a NMOS structure having a drain diffusion region 14b with a first drain diffusion n+ and a special

second drain diffusion p 40 as disclosed in Col. 5, lines 41-44, lines 48-49 and Fig. 5.

Both teachings are analogous electrostatic discharge protection circuits for protecting semiconductor devices in an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al., which teaches a first and a special second drain diffusion, into the protection circuit of the applicant's acknowledged prior art because p+ pocket implantation have extra function of reducing the breakdown voltage and create junction breakdown much earlier during an ESD event.

With respect to claim 2, applicant's acknowledged prior art teaches that the protection discharging means [Fig. 1A, 7] further comprises a resistor [Fig. 1A, R].

With respect to claim 4, applicant's prior art teaches that the gate of said discharging NMOS device is connected to the first end of said resistor and the second end of said resistor is connected to said second voltage source [Fig. 1A, Vss].

With respect to claim 5, Chen et al. teaches a NMOS transistor having a drain wherein first drain diffusion is a n+ donor diffusion to form a normal NMOS drain region [Col. 5, lines 48-49 and Fig. 5].

With respect to claim 6, Chen et al. teaches a NMOS transistor having a drain wherein said special second drain diffusion [Fig. 5, 40] is of opposite

dopent p+ than said first drain diffusion n+ and extends under and around said normal drain region [Col. 5, lines 41-44, 48-49 and Fig. 5].

With regard to the limitation of a resistor value between 1 and 100 K ohms in claim 7, a resistance value between 1 and 100 K ohms is very common in the art. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 8, applicant's prior art teaches that the switching circuit string 6 provides a driving current to the output pad [Fig. 1A, 8].

With respect to claim 9, applicant's prior art teaches that the driving current is determined by the total number of the switching strings as disclosed in Fig. 1A. With regard to the limitation of current between 2 and 48 ma, this range does not differ from conventional practice in the art of solid state device fabrication. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With regard to the limitation of voltage source between 2.5 and 5 volts in claim 10, a voltage source between 2.5 and 5 is the standard across the electronics industry. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover

Art Unit: 2836

the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 11, applicant's prior art teaches that the second voltage source [Fig. 1A, Vss].

With respect to claim 24, applicant's prior art teaches that the ESD protection discharging means comprises discharging NMOS device [Fig. 1A, 7] and a resistor. With regard to the limitation of a resistor value between 1 and 100 K ohms in claim 24, a resistance value between 1 and 100 K ohms is very common in the art. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). However, the prior art fails to teach or suggest a discharging NMOS device with a special diffusion region under and around said device normal drain region of opposite dopant than said normal drain region.

Chen et al. teaches electrostatic discharge protection devices that have islands and breakdown-enhanced layers. Chen et al. teaches a NMOS structure having a drain diffusion region 14b with a first drain diffusion n+ and a special second drain diffusion p 40 as disclosed in Col. 5, lines 41-44, lines 48-49 and Fig. 5.

Both teachings are analogous electrostatic discharge protection circuits for protecting semiconductor devices in an integrated circuit. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al., which teaches a first and a special second drain diffusion, into the protection circuit of the applicant's acknowledged prior art because p+ pocket implantation have extra function of reducing the breakdown voltage and create junction breakdown much earlier during an ESD event.

With respect to claim 25, applicant's prior art teaches that ESD protection discharging means is connected to the circuits to be protected by connecting said drain of said discharging NMOS device to said first voltage source [Fig. 1A, Vcc] and connecting the source of said discharging NMOS to said second voltage source [Fig. 1A, Vss].

With respect to claim 26, applicant's prior art teaches that ESD protection discharging means [Fig. 1A, Transistor] is connected to the circuits to be protected by connecting the gate of said discharging NMOS device to the first end of said resistor [Fig. 1A, R] and connecting the second end of said resistor [Fig. 1A, R] to said second voltage source [Fig. 1A, Vss].

With regard to the limitation of boron with a dosage between $1\text{E}13$ and $1\text{E}14$ a/cm² and dopent concentration between $1\text{E}16$ and $1\text{E}19$ a/cm² in claim 27, the concentrations do not differ from conventional practice in the art of solid state device fabrication. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With regard to the limitation of voltage source between 2.5 and 5 volts in claim 28, the voltage source does not differ from conventional practice in the art of solid-state device fabrication. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 29, applicant's prior art teaches that the second voltage source designated V_{ss} [Fig. 1A, V_{ss}] is connected to a voltage level below V_{cc} , typically ground Fig. 1A].

With respect to claim 30, applicant's prior art teaches that the separate logic signal lines are connected to internal logic devices [Fig. 1A].

8. Claims 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Jung, Patent No. 5,932,916. With respect to claim 12, applicant's prior art teaches an effective V_{cc} to V_{ss} power ESD protection device between V_{cc} and V_{ss} power bus lines that comprises a silicon substrate 10 having a first dopent type; field oxide regions 12 with the substrate for isolation of said ESD protection device; a FET gate 16 with abutting spacers 18 for the ESD protection device; multiple regions of a second dopent type 22, 24 of opposite dopent to the substrate 10 for the ESD protection device between the gate 16 and the field oxide regions 12; a protective insulation layer 20 over the ESD protection device; and first 16, second 22, and third 24 electrical conductor elements.

However, the prior art fails to teach or suggest multiple regions of a third dopent type of opposite dopent to the substrate for the ESD protection device between the gate and the field oxide regions; and a special fourth dopent region of similar dopent to the substrate beneath one said second and third dopent region.

Jung teaches an electrostatic discharge protection circuit that comprises a P-type substrate 50 having a first dopent type; multiple regions 51 and 57 of a second dopent type of opposite dopent to the substrate for the ESD protection device; multiple regions 52 and 56 of a third dopent type of opposite dopent to the substrate for the ESD protection device; and a special fourth dopent region 53 of similar dopent to the substrate as disclosed in Col. 4, lines 41-44, lines 48-49 and Fig. 4B.

Both teachings are analogous electrostatic discharge protection circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jung, which teaches four dopent regions, into the ESD protection circuit of the applicant's acknowledged prior art to maximize the efficiency in ESD protection by reducing the triggering voltage using a control gate and floating gate.

With regard to the limitation of dopent concentration in claims 13 and 17-19, the concentrations do not differ from conventional practice in the art of solid state device fabrication. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover

the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to the limitation of gate oxide insulator thickness in claims 14 and 15, the thickness does not differ from conventional practice in the art of solid state device fabrication. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 16, applicant's prior art teaches that the FET gate abutting spacers 18 are of silicon oxide as disclosed in the Specification, Page 2, line 18 and Fig. 1B.

With respect to claim 20, applicant's prior art teaches that the drain electrical conductor element is connected to a first voltage source V_{cc} , and the source electrical conductor element is connected to a second voltage source V_{ss} as disclosed in Fig. 1A.

With respect to claim 21, applicant's prior art teaches that the gate electrical conductor element is connected to the first end of a diffused resistor as disclosed in Fig. 1A. With regard to the limitation of a resistor value between 1000 and 100 K ohms, a resistance value between 1000 and 100 K ohms is very common in the art. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover

the optimum or workable ranges by routine experiment. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 22, applicant's prior art teaches that the second end of the resistor is connected to the second voltage source Vss or ground as disclosed in Fig. 1A.

Response to Arguments

9. With regard to the arguments about withdrawing a double patenting rejection, a double patenting rejection is still valid with regard to claim 23, since it is an exact duplicate of claim 1 of Patent NO. 6,682,993.

With regard to the arguments about claim 1, it is believed that the applicant's acknowledged prior art combined with Chen et al. [PN. 6,858,900] reads on the claim limitation "wherein said protection discharging means comprising a discharging NMOS device with a first and a second drain diffusion, the drain of said discharging NMOS device is directly connected to said first voltage source, and the source of said discharging NMOS device is directly connected to said second voltage source."

With regard to the arguments about claim 23, the acknowledged prior art [Fig. 1A] still reads on claim 23 with the added limitation of "and further directly connected to." The ESD discharging means [Fig. 1A, transistor] for discharging ESD energy appearing between and further directly connected to said first and second voltage source [Fig. 1A, Vcc and Vss] as disclosed in Fig. 1A.

With regard to the arguments about claim 12, the specification does not contain support for the claim limitations [claim 12, lines 10-13, multiple regions of a third dopant region and a special fourth dopant region]. The limitations of claim 12 should be addressed to account for this. Based on examiner's best understanding, it is believed that prior art [Jung, Patent No. 5,932,916] reads on the claim limitations of claim 12.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2836

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
11/09/2005



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